INSTITUT TEKNOLOGI SEPULUH NOPEMBER (ITS)
FAKULTAS TEKNOLOGI ELEKTRO DAN INFORMATIKA CERDAS
DEPARTEMEN TEKNIK ELEKTRO
Program Studi Sarjana (S1) Teknik Telekomunikasi

1	**Nama Mata Kuliah / Course Name**	:	Sistem Tertanam dalam Telekomunikasi / *Embedded Systems in Telecommunications*
2	**Kode Mata Kuliah / Course Code**	:	EL234405
3	**Kredit / Credits**	:	3 SKS
4	**Semester / Semester**	:	4

Deskripsi Mata Kuliah / Course Description

Mata kuliah ini mempelajari tentang implementasi rangkaian dan sistem digital menggunakan komponen hardware terprogram FPGA, yang juga meliputi prosedur perancangan menggunakan Bahasa HDL (Hardware Description Language) seperti VHDL atau Verilog, serta penggunaan EDA tools untuk perancangannya. Implementasi mencakup perancangan rangkaian kombinasional, rangkaian sekuensial, FSM, rangkaian DSP filter digital.

This course studies the implementation of digital circuits and systems using FPGA programmed hardware components, which also includes design procedures using HDL (Hardware Description Language) languages such as VHDL or Verilog, and the use of EDA tools for design. Implementation includes the design of combinational circuits, sequential circuits, FSM, digital DSP filter circuits.

Capaian Pembelajaran Lulusan (CPL) Yang Dibebankan Mata Kuliah / Program Learning Outcomes Charged to The Course

1. (CPL-05) Mampu merancang komponen, sistem, dan proses yang logis dan realistis sesuai dengan spesifikasi yang ditentukan dengan mempertimbangkan aspek keselamatan, sosial, budaya, lingkungan, dan ekonomi.
   (PLO-05) Able to design logical and realistic components, systems and processes in accordance with the specified specifications by considering safety, social, cultural, environmental and economic aspects.

2. (CPL-07) Mampu mengidentifikasi, memformulasikan, menganalisis, dan menyelesaikan permasalahan kompleks di bidang teknik telekomunikasi
   (PLO-07) Able to identify, formulate, analyze, and solve complex problems in the field of telecommunications engineering

3. (CPL-08) Mampu mengetahui dan mengaplikasi metode dan keahlian sesuai perkembangan terkini di bidang ilmu pengetahuan dan teknologi untuk

menyelesaikan permasalahan di bidang Teknik Telekomunikasi dengan mengedepankan nilai-nilai universal
(PLO-08) Able to know and apply methods and expertise according to the latest developments in the field of science and technology to solve problems in the field of Telecommunication Engineering by prioritizing universal values

Capaian Pembelajaran Mata Kuliah / Course Learning Outcomes

1. Mampu memahami sistem digital: kombinasional, sekuensial, dan Finite State Machine (FSM) / *Able to understand digital systems: combinational, sequential, and Finite State Machine (FSM).*
2. Mampu memahami evolusi dan arsitektur Komponen Hardware Programmable: PROM, PAL, PLA, Masked Gate Array, CPLD, FPGA / *Able to understand the evolution and architecture of Programmable Hardware Components: PROM, PAL, PLA, Masked Gate Array, CPLD, FPGA*
3. Mampu menerapkan penggunaan EDA Tools (Quartus Altera atau ISE Xilinx): Editing, Test bench, Synthesis, Place and route Programming tools / *Able to apply the use of EDA Tools (Quartus Altera or Xilinx ISE): Editing, Test bench, Synthesis, Place and route Programming tools.*
4. Mampu merancang rangkaian digital menggunakan Hardware Description Language (HDL) berupa VHDL atau verilog dengan menggunakan representasi arsitektur persamaan logika/Boolean, data flow dan behavioral, dan mengetahui cara melakukan verifikasi: Simulation, Timing analysis / *Able to design digital circuits using Hardware Description Language (HDL) in the form of VHDL or verilog using architectural representations of logic/Boolean equations, data flow and behavior, and know how to verify: Simulation, Timing analysis.*
5. Mampu merancang rangkaian kombinasional dan rangkaian sekuensial menggunakan HDL dan mengimplementasikan ke dalam FPGA (pin planner, programmer ke FPGA) / *Able to design combinational circuits and sequential circuits using HDL and implement them into FPGA (pin planner, programmer to FPGA)*
6. Mampu merancang rangkaian filter digital untuk pengolahan sinyal digital menggunakan HDL dan mengimplementasikan ke dalam FPGA (pin planner, programmer ke FPGA) / *Able to design digital filter circuits for digital signal processing using HDL and implement them into FPGA (pin planner, programmer to FPGA)*

Pokok Bahasan / Contents

1. Sistem Digital: kombinasional, sekuensial, Finite State Machine (FSM) / *Digital Systems: combinational, sequential, Finite State Machine (FSM)*
2. Evolusi dan Arsitektur komponen Hardware terprogram: PROM, PAL, PLA, Masked Gate Array, FPGA / *Evolution and Architecture of programmable Hardware components: PROM, PAL, PLA, Masked Gate Array, FPGA*
3. EDA Tools (Quartus Altera atau ISE Xilinx): Editing, Test bench, Synthesis, Place and route, Programming tools / *EDA Tools (Quartus Altera or ISE Xilinx): Editing, Test bench, Synthesis, Place and route, Programming tools*
4. Desain teknik menggunakan HDL (VHDL atau verilog), meliputi Spesifikasi, pemilihan komponen, perancangan sistem, pembuatan entity dan arsitektur

dengan metode persamaan logika/Boolean, data flow dan behavioral, verifikasi: Simulation, Timing analysis, implementasi dan test / *Engineering design using HDL (VHDL or verilog), including specifications, component selection, system design, entity creation and architecture using the logic/Boolean equation method, data flow and behavior, verification: Simulation, Timing analysis, implementation and test*

5. Implementasi Rangkaian Kombinasional dan Rangkaian Sekuensial perancangan komponen terprogram ke dalam FPGA / *Implementation of Combinational Circuits and Sequential Circuits designing programmed components into FPGAs*
6. Implementasi Sistem Digital dan pengolahan sinyal digital (Digital Filter) perancangan komponen terprogram ke dalam FPGA */ Implementation of Digital Systems and digital signal processing (Digital Filter) design of components programmed into the FPGA*

Prasyarat / Pre-requisite

Sistem Digital / *Digital System*

Pustaka / Reference

Utama / Primary :

1. M Bob Zeidman, Designing with FPGAs and CPLDs, Elsevier, 2002
2. Kevin Skahill, VHDL for Programmable Logic, Addison Wesley, 1996
3. S. Brown and Z. Vranesic: Fundamentals of Digital Logic and VHDL Design, 3rd Edition McGraw-Hill, 2009.

Pendukung / Support :

1. Enoch O. Hwang, Digital Logic and Microprocessor Design with VHDL, CL-Engineering, 2006 atau 2016 yang terbaru.
2. M. Morris Mano and Charles R. Kimme, Logic and Computer Design Fundamentals, 4th edition, Pearson Prentice Hall, 2008.