INSTITUT TEKNOLOGI SEPULUH NOPEMBER (ITS)
FAKULTAS TEKNOLOGI ELEKTRO DAN INFORMATIKA CERDAS
DEPARTEMEN TEKNIK ELEKTRO
Program Studi Sarjana (S1) Teknik Elektro

INSTITUT TEKNOLOGI SEPULUH NOPEMBER (ITS)
FACULTY OF INTELLIGENT ELECTRICAL & INFORMATICS TECHNOLOGY
DEPARTMENT OF ELECTRICAL ENGINEERING
Bachelor Degree Program in Electrical Engineering

1	**Nama Mata Kuliah / *Course Name***	:	Perancangan Komponen Terprogram / *Design Using Programmable Devices*
2	**Kode Mata Kuliah / *Course Code***	:	EE234553
3	**Kredit / *Credits***	:	2 SKS
4	**Semester / *Semester***	:	5

Deskripsi Mata Kuliah / *Course Description*

Mata kuliah ini mempelajari tentang implementasi rangkaian dan sistem digital menggunakan komponen hardware terprogram FPGA, yang juga meliputi prosedur perancangan menggunakan Bahasa HDL (Hardware Description Language) seperti VHDL atau Verilog, serta penggunaan EDA tools untuk perancangannya. Implementasi mencakup perancangan rangkaian kombinasional, rangkaian sekuensial, FSM, rangkaian DSP filter digital. / *This course covers the implementation of digital circuits and systems using programmable hardware components like FPGA. It also includes the design process using Hardware Description Languages (HDL) such as VHDL or Verilog, as well as the use of Electronic Design Automation (EDA) tools for the design. The implementation encompasses the design of combinational circuits, sequential circuits, finite state machines (FSM), and digital signal processing (DSP) digital filter circuits.*

Capaian Pembelajaran Lulusan (CPL) Yang Dibebankan Mata Kuliah / *Program Learning Outcomes Charged to The Course*

CPL 1 Mampu menunjukkan sikap dan karakter yang mencerminkan: ketakwaan kepada Tuhan Yang Maha Esa, etika dan integritas, berbudi pekerti luhur, peka dan peduli terhadap masalah sosial dan lingkungan, menghargai perbedaan budaya dan kemajemukan, menjunjung tinggi penegakan hukum mendahulukan kepentingan bangsa dan masyarakat luas, melalui kreatifitas dan inovasi, ekselensi, kepemimpinan yang kuat, sinergi, dan potensi lain yang dimiliki untuk mencapai hasil yang maksimal / *Being able to demonstrate attitudes and characteristics that reflect: devotion to the One Almighty God, ethics and*

integrity, noble virtues, sensitivity and care towards social and environmental issues, appreciation of cultural diversity and inclusivity, upholding the rule of law with a priority on the interests of the nation and the wider community, through creativity and innovation, excellence, strong leadership, synergy, and other potentials possessed to achieve maximum results.

CPL 5 Mampu mendesain komponen, sistem, dan proses yang logis dan realistis sesuai dengan spesifikasi yang ditentukan dengan mempertimbangkan aspek keselamatan, sosial, budaya, lingkungan, dan ekonomi / *Able to design components, systems, and processes that are logical and realistic in accordance with specified specifications, while considering safety, social, cultural, environmental, and economic aspects.*

CPL 6 Mampu mengkaji dan memanfaatkan matematika, ilmu pengetahuan alam dan teknologi serta mengidentifikasi, memformulasikan dan menyelesaikan permasalahan di bidang teknik elektro / *Able to evaluate and utilize mathematics, natural sciences, and technology, as well as identify, formulate, and solve problems in the field of electrical engineering.*

CPL 9 Mampu berkomunikasi secara efektif baik dalam bentuk tulisan maupun lisan / *Able to effective communication, both in written and oral forms.*

Capaian Pembelajaran Mata Kuliah / *Course Learning Outcomes*

1. Mampu memahami sistem digital: kombinasional, sekuensial, dan Finite State Machine (FSM). / *Able to understand digital systems: combinational, sequential, and Finite State Machines (FSM).*
2. Mampu memahami evolusi dan arsitektur Komponen Hardware Programmable: PROM, PAL, PLA, Masked Gate Array, CPLD, FPGA. */ Able to understand the evolution and architecture of Programmable Hardware Components: PROM, PAL, PLA, Masked Gate Array, CPLD, FPGA.*
3. Mampu menerapkan penggunaan EDA Tools (Quartus Altera atau ISE Xilinx): Editing, Test bench, Synthesis, Place and route Programming tools. / *Capable of using Electronic Design Automation (EDA) Tools (such as Quartus Altera or ISE Xilinx): Editing, Test bench, Synthesis, Place and route programming tools.*
4. Mampu merancang rangkaian digital menggunakan Hardware Description Language (HDL) berupa VHDL atau verilog dengan menggunakan representasi arsitektur persamaan logika/Boolean, data flow dan behavioral, dan mengetahui cara melakukan verifikasi: Simulation, Timing analysis. / *Able to design digital circuits using Hardware Description Language (HDL) such as VHDL or Verilog, utilizing logic/Boolean equation architecture, data flow, and behavioral representation, and knowing how to perform verification: Simulation, Timing analysis.*
5. Mampu merancang rangkaian kombinasional dan rangkaian sekuensial menggunakan HDL dan mengimplementasikan ke dalam FPGA (pin planner, programmer ke FPGA) / *Capable of designing combinational and sequential circuits using HDL and implementing them into an FPGA (pin planner, programming to FPGA).*
6. Mampu merancang rangkaian filter digital untuk pengolahan sinyal digital menggunakan HDL dan mengimplementasikan ke dalam FPGA (pin planner,

programmer ke FPGA) / *Able to design digital filter circuits for digital signal processing using HDL and implementing them into an FPGA (pin planner, programming to FPGA).*

Pokok Bahasan / *Contents*

1. Sistem Digital: kombinasional, sekuensial, Finite State Machine (FSM) / *Digital Systems: combinational, sequential, Finite State Machine (FSM)*
2. Evolusi dan Arsitektur komponen Hardware terprogram: PROM, PAL, PLA, Masked Gate Array, FPGA / *Evolution and architecture of programmable hardware components: PROM, PAL, PLA, Masked Gate Array, FPGA*
3. EDA Tools (Quartus Altera atau ISE Xilinx): Editing, Test bench, Synthesis, Place and route, Programming tools / *EDA Tools (Quartus Altera or ISE Xilinx): Editing, Test bench, Synthesis, Place and route, Programming tools*
4. Desain teknik menggunakan HDL (VHDL atau verilog), meliputi Spesifikasi, pemilihan komponen, perancangan sistem, pembuatan entity dan arsitektur dengan metode persamaan logika/Boolean, data flow dan behavioral, verifikasi: Simulation, Timing analysis, implementasi dan test / *Design techniques using HDL (VHDL or Verilog), including Specification, component selection, system design, entity creation, and architecture using methods of logic/Boolean equations, data flow, and behavioral, verification: Simulation, Timing analysis, implementation, and testing*
5. Implementasi Rangkaian Kombinasional dan Rangkaian Sekuensial perancangan komponen terprogram ke dalam FPGA / *Implementation of Combinational Circuits and Sequential Circuits for programmable component design into FPGA*
6. Implementasi Sistem Digital dan pengolahan sinyal digital (Digital Filter) perancangan komponen terprogram ke dalam FPGA / *Implementation of Digital Systems and digital signal processing (Digital Filter) for programmable component design into FPGA*

Prasyarat / *Pre-requisite*

Sistem Digital dan Mikroprosesor / *Microprocessor and Microcontroller Systems*

Pustaka / *Reference*

1. M Bob Zeidman, Designing with FPGAs and CPLDs, Elsevier, 2002
2. Kevin Skahill, VHDL for Programmable Logic, Addison Wesley, 1996
3. S. Brown and Z. Vranesic: Fundamentals of Digital Logic and VHDL Design, 3rd Edition McGraw-Hill, 2009.