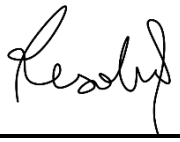
MODULE HANDBOOK
DIGITAL TECHNIQUES AND LABORATORY

BACHELOR DEGREE PROGRAM
DEPARTMENT OF BIOMEDICAL ENGINEERING
FACULTY OF INTELLIGENT ELECTRICAL AND INFORMATICS TECHNOLOGY

INSTITUT TEKNOLOGI SEPULUH NOPEMBER

ENDORSEMENT PAGE

	MODULE HANDBOOK **Digital Techniques and Laboratory** **DEPARTMENT OF BIOMEDICAL ENGINEERING** **INSTITUT TEKNOLOGI SEPULUH NOPEMBER** **Number :** B/21354/IT2.IX.5.1.2/PP.03.00.00/2020

Proses ***Process***	**Penanggung Jawab** ***Person in Charge***			**Tanggal** ***Date***
	Nama ***Name***	**Jabatan** ***Position***	**Tandatangan** ***Signature***	
Perumus *Preparation*	Dr. Tri Arief Sardjono, S.T., M.T.	Dosen *Lecturer*		**November 23, 2019**
Pemeriksa dan Pengendalian *Review and Control*	Ir. Josaphat Pramudijanto, M.Eng.	Tim kurikulum *Curriculum team*		**February 11, 2020**
Persetujuan *Approval*	Dr. Rachmad Setiawan, S.T., M.T.	Koordinator RMK *Course Cluster Coordinator*		**March 03, 2020**
Penetapan *Determination*	Dr. Achmad Arifin, S.T., M.Eng.	Kepala Departemen *Head of Department*		**March 10, 2020**

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MODULE HANDBOOK

DIGITAL TECHNIQUES AND LABORATORY

Module name	**Digital Techniques and Laboratory**	
Module level	Undergraduate	
Code	EB184405	
Course (if applicable)	Digital Techniques and Laboratory	
Semester	Fourth Semester (Even)	
Person responsible for the module	Dr. Tri Arief Sardjono, S.T., M.T.	
Lecturer		
Language	Bahasa Indonesia and English	
Relation to curriculum	Undergradute degree program, **mandatory**, 4th semester	
Type of teaching, contact hours	Lectures, <60 students	
Workload	1. Lectures : 4 x 50 = 200 minutes per week. 2. Exercises and Assignments : 4 x 50 = 200 minutes per week. 3. Private learning : 4 x 50 = 240 minutes per week.	
Credit points	4 credit points (sks)	
Requirements according to the examination regulations	A student must have attended at least 75% of the lectures to sit in the exams.	
Mandatory prerequisites	-	
Learning outcomes and their corresponding PLOs	Course Learning Outcome (CLO) after completing this module, CLO 1: Students are able to understand and explain basic theories of digital electronic systems such as the difference between analog systems and digital systems, number systems and coding systems. CLO 2: Students are able to understand and explain about logic gates, Boolean algebra, simplification of logic equations and be able to do experiments related to basic logic gate circuits. CLO 3: Students are able to understand, explain, and analyze combinational logic and be able to do experiment with combinational logic sequences.	PLO-02 PLO-03 PLO-03 PLO-03

	CLO 4: Students are able to understand, explain, explain, and analyze sequential logic and be able to do experiment with sequential logic circuits. CLO 5: Students are able to understand and explain the stages of designing a digital-based Programmable Logic Device (PLD) system and be able to realize it.	PLO-05
Content	This course is a mandatory course that discuss the basic science of digital system both in theoru and practice. This course aims to make students understand about number system theory, logic gates, combinational circuits, multivibrator circuits, sequential circuits, and programmable logic decvices and their applications. In addition, this course also aims to allow students to experiment on the theory that has been studied and understood, so that students can be trained and skilled in performing analysis, designing digital systems and using tools or tools with the correct procedures. With the understanding of theory and skills in the laboratory, students are expected to be able to apply it especially to biomedical disciplines.	
Study and examination requirements and forms of examination	• In-class exercises • Assignment 1, 2, 4, 5, 6, 7, 8 • Lab work 1, 2, 3, 4 • Mid-term examination • Final examination	
Media employed	LCD, whiteboard, websites (myITS Classroom), zoom.	
Reading list	Main: 1. S John F. Wakerly, “Digital Design : Principles & Practices 3rd Edition”, Prentice Hall, 1999. 2. David M., H., and Sarah L. Harris, “Digital Design and Computer Architecture 1st Edition”, Elsevier Inc, 2007. 3. Richard F. T, “Engineering Digital Design Second Edition”, Academic Press, 2000. 4. Bob Zeidman, “Designing with FPGAs and CPLDs”, Elsevier, 2002. 5. Kevin Skahill,“VHDL for Programmable Logic”, Addison Wesley, 1996	

I. Rencana Pembelajaran Semester / *Semester Learning Plan*

	INSTITUT TEKNOLOGI SEPULUH NOPEMBER (ITS) **FAKULTAS TEKNOLOGI ELEKTRO DAN INFORMATIKA CERDAS** **DEPARTEMEN TEKNIK BIOMEDIK**	**Kode Dokumen**

RENCANA PEMBELAJARAN SEMESTER

MATA KULIAH (MK) ***COURSE***	**KODE** ***CODE***	**Rumpun MK** ***Course Cluster***	**BOBOT (sks)** **Credits**		**SEMESTER**	**Tgl Penyusunan** ***Compilation Date***
Digital Techniques and Laboratory	EB184405	Biomedical Instrumentation and Signal Processing	T=4	P=0	IV	15 Juni 2020

OTORISASI / PENGESAHAN ***AUTHORIZATION / ENDORSEMENT***	**Dosen Pengembang RPS** ***Developer Lecturer of Semester Learning Plan***	**Koordinator RMK** ***Course Cluster Coordinator***	**Ka DEPARTEMEN** ***Head of Department***
	(Dr. Tri Arief Sardjono, S.T., M.T.)	**(Dr. Rachmad Setiawan, S.T., M.T.)**	**(Dr. Achmad Arifin, S.T., M.Eng.)**

Capaian Pembelajaran ***Learning Outcomes***	**CPL-PRODI yang dibebankan pada MK** ***PLO Program Charged to The Course***	
	CPL-02 ***PLO-02***	Mampu **menemukan**, **memahami**, **menjelaskan**, **merumuskan**, dan **menyelesaikan** permasalahan umum pada bidang Teknik dan permasalahan khusus pada bidang Teknik Biomedika yang meliputi instrumentasi biomedika cerdas, teknik rehabilitasi medika, pencitraan dan pengolahan citra medika, serta informatika medika *Able to **find**, **understand**, **explain**, **formulate**, and **solve** general problems in the field of Engineering and special problems in the field of Biomedical Engineering which includes intelligent biomedical instrumentation, medical rehabilitation techniques, imaging and processing of medical images, and medical informatics*
	CPL-03	Mampu **merancang** dan **melaksanakan** eksperimen laboratorium dan/atau lapangan, **menganalisa** dan **menginterpretasi** data, serta menggunakan penilaian yang obyektif untuk menarik kesimpulan

	PLO-03	*Able to **design** and **implement** laboratory experiment and / or field experiments, **analyze** and **interpret** data, and use objective assessments to draw conclusions.*
	CPL-05	Mampu **mendesain** komponen, sistem, dan proses dalam bidang Teknik Biomedika yang sistematis, logis, dan realistis sesuai dengan spesifikasi yang ditentukan dengan mempertimbangkan aspek keselamatan, sosial, budaya, lingkungan, dan ekonomi dengan **mengenali/memanfaatkan** sumber daya lokal dan nasional dengan wawasan global
	PLO-05	*Able to **design** components, systems, and processes in the field of Biomedical Engineering that are systematic, logical, and realistic appropriate with specified specifications by considering aspects of safety, social, cultural, environmental, and economic by **recognizing / utilizing** local and national resources with global insight*
	Capaian Pembelajaran Mata Kuliah (CPMK) – Bila CP MK sebagai kemampuan pada tiap tahap pembelajaran CP MK = Sub CP MK ***Course Learning Outcome (CLO) - If CLO as description capability of each Learning Stage in the course, then CLO = LLO***	
	CP MK 1	Mahasiswa mampu memahami dan menjelaskan teori dasar sistem elektronika digital seperti perbedaan antara sistem analog dan sistem digital, sistem bilangan dan sistem pengkodean.
	CLO 1	*Students are able to understand and explain basic theories of digital electronic systems such as the difference between analog systems and digital systems, number systems and coding systems.*
	CP MK 2	Mahasiswa mampu memahami dan menjelaskan tentang gerbang logika, aljabar boolean, penyederhanaan persamaan logika serta mampu melakukan ekperimen berkaitan dengan rangkaian dasar gerbang logika.
	CLO 2	*Students are able to understand and explain about logic gates, Boolean algebra, simplification of logic equations and be able to do experiments related to basic logic gate circuits.*
	CP MK 3	Mahasiswa mampu memahami, menjelaskan, merancang dan menganalisa rangkaian logika kombinasional serta mampu melakukan ekperimen berkaitan dengan rangkaian logika kombinasional.
	CLO 3	*Students are able to understand, explain, design and analyze a combination of combinational logic and are able to experiment with a combination of combinational logic.*
	CP MK 4	Mahasiswa mampu memahami, menjelaskan, merancang dan menganalisa rangkaian logika sekuensial serta mampu melakukan ekperimen berkaitan dengan rangkaian logika sekuensial.
	CLO 4	*Students are able to understand, explain, design and analyze sequential logic circuits and be able to do experiments related to sequential logic circuits.*

	CP MK 5 ***CLO 5***	Mahasiswa mampu memahami dan menjelaskan tahapan perancangan sistem berbasis digital *Programmable Logic Device* (PLD) serta mampu merealisasikannya. *Students are able to understand and explain the stages of designing a digital-based Programmable Logic Device (PLD) system and be able to realize it.*

Peta CPL – CP MK

Map of PLO - CLO

	CPL-01	CPL-02	CPL-03	CPL-04	CPL-05	CPL-06	CPL-07	CPL-08	CPL-09	CPL-10	CPL-11	CPL-12
CPMK 1 / SUB CPMK 1 *CLO 1 / LLO 1*		√										
CPMK 2 / SUB CPMK 2 *CLO 2 / LLO 2*			√									
CPMK 3 / SUB CPMK 3 *CLO 3 / LLO 3*			√									
CPMK 4 / SUB CPMK 4 *CLO 4 / LLO 4*			√									
CPMK 5 / SUB CPMK 5 *CLO 5 / LLO 5*					√							

Diskripsi Singkat MK ***Short Description of Course***	Mata kuliah Teknik Digital dan Laboratorium merupakan mata kuliah wajib yang membahas ilmu dasar sistem digital baik secara teori maupun praktek. Mata kuliah ini bertujuan agar mahasiswa memahami tentang teori sistem bilangan, gerbang logika, rangkaian kombinasional, rangkaian multivibrator, rangkaian sekuensial, dan programmable logic decvice serta aplikasinya. Selain itu, mata kuliah ini juga bertujuan agar mahasiswa mampu melakukan eksperimen mengenai teori yang sudah dipelajari dan dipahami, sehingga mahasiswa bisa terlatih dan terampil dalam melakukan analisa, perancangan sistem digital serta menggunakan peralatan atau tools dengan prosedur yang benar. Dengan pemahaman teori dan keterampilan dalam laboratorium tersebut, mahasiswa diharapkan mampu menerapkannya terutama pada disiplin ilmu biomedik. *This course is a mandatory course that discuss the basic science of digital system both in theoru and practice. This course aims to make students understand about number system theory, logic gates, combinational circuits, multivibrator circuits, sequential circuits, and programmable logic decvices and their applications. In addition, this course also aims to allow students to experiment on the theory that has been studied and understood, so that students can be trained and skilled in performing analysis, designing digital systems and using tools or tools with the correct procedures. With the understanding of theory and skills in the laboratory, students are expected to be able to apply it especially to biomedical disciplines.*

Bahan Kajian: Materi pembelajaran ***Course Materials:***	1. Baris Bilangan / *Number Line* 2. Gerbang Logika / *Logic Gate* 3. Rangkaian Kombinasional / *Combinational Circuits* 4. Penyederhanaan Rangkaian Kombinasional / *Simplification of Combinational Circuits* 5. Multivibrator/ *Multivibrator* 6. Rangkaian Sekuensial / *Sequential Circuits* 7. Bahasa Deskripsi Hardware / *Hardware Description Language*
Pustaka ***References***	**Utama / *Main*:** 1. S John F. Wakerly, "Digital Design : Principles & Practices 3rd Edition", Prentice Hall, 1999. 2. David M., H., and Sarah L. Harris, "Digital Design and Computer Architecture 1st Edition", Elsevier Inc, 2007. 3. Richard F. T, "Engineering Digital Design Second Edition", Academic Press, 2000. 4. Bob Zeidman, "Designing with FPGAs and CPLDs", Elsevier, 2002. 5. Kevin Skahill,"VHDL for Programmable Logic", Addison Wesley, 1996
Dosen Pengampu ***Lecturers***	
Matakuliah syarat ***Prerequisite***	-

Mg Ke/ ***Week***	**Kemampuan akhir tiap tahapan belajar (Sub-CPMK) /** ***Final ability of each learning stage (LLO)***	**Penilaian /** ***Assessment***		**Bantuk Pembelajaran; Metode Pembelajaran; Penugasan Mahasiswa; [Estimasi Waktu] /** ***Form of Learning; Learning Method; Student Assignment; [Estimated Time]***		**Materi Pembelajaran [Pustaka] /** ***Learning Material [Reference]***	**Bobot Penilaian /*Assess-ment Load* (%)**
		Indikator / ***Indicator***	**Kriteria & Teknik/** ***Criteria & Techniques***				
(1)	**(2)**	**(3)**	**(4)**	**Tatap Muka /** ***In-class* (5)**	**Daring /** ***Online* (6)**	**(7)**	**(8)**

1,2	Mahasiswa mampu memahami dan menjelaskan teori dasar sistem elektronika digital seperti perbedaan antara sistem analog dan sistem digital, sistem bilangan dan sistem pengkodean *Students are able to understand and explain basic theories of digital electronic systems such as the difference between analog systems and digital systems, number systems and coding systems.*	• Memahami dan mampu menjelaskan teori dasar teknik digital • Memahami dan mampu menjelaskan sistem bilangan dan sistem pengkodean • Mampu menghitung konversi bilangan, aritmatika biner, komplemen bilangan biner, bilangan bertanda dan operasinya, dan sistem pengkodean. • *Understand be able to explain the basic theory of digital technique* • *Understand be able to explain number systems and coding system* • *Able to calculate the conversion of numbers, binary arithmetic, binary number complement, marked numbers and*	**Non-Tes** **Tugas 1:** • Mengerjakan soal perhitungan mengenai konversi bilangan, aritmatika biner, komplemen bilangan biner, bilangan bertanda dan operasinya, dan sistem pengkodean (Tugas Tertulis) ***Non-Test*** ***Task 1:*** • *Doing calculation problems about number conversion, binary arithmetic, binary number complement, marked numbers and their operations, and coding systems (Written Tasks)*	• Kuliah, diskusi dan tugas. [TM : 2 x (4 x 50")] [BM : 2 x (4 x 50")] [PT : 2 x (4 x 50")] • *Lectures discussion and assignment.* *[FF : 2 x (4 x 50")]* *[SS : 2 x (4 x 50")]* *[SA : 2 x (4 x 50")]*	• Chatting dan diskusi dalam forum platform ITS. • *Chat and discussion in ITS platform forum*	• Pengenalan teknik digital : kuantitas digital dan analog, binary digit, level logika, digital waveform, pengenalan fungsi logika dasar. • Sistem bilangan dan sistem pengkodean : bilangan decimal dan biner, konversi decimal ke biner, aritmatika biner, komplemen bilangan biner, bilangan bertanda dan operasinya, bilangan heksadesimal dan octal, binary code decimal (BCD), digital codes, error codes • *Introduction to digital techniques: digital and analog quantity, binary digits, logic level,*	**Tugas 1 /** ***Task 1:*** **2.5**

		their operations, and coding systems.				*digital waveform, introduction of basic logic functions.* • *Number systems and coding systems: decimal and binary numbers, decimal to binary conversion, binary arithmetic, binary number complement, marked numbers and their operations, hexadecimal and octal numbers, binary code decimal (BCD), digital codes, error codes.*	
3-5	Mahasiswa mampu memahami dan menjelaskan tentang gerbang logika, aljabar boolean, penyederhanaan persamaan logika serta mampu melakukan ekperimen	• Memahami dan mampu menjelaskan mengenai gerbang logika dan aljabar Boolean. • Mampu menyelesaikan	**Non-tes :** **Tugas 2:** • Mengerjakan soal perhitungan mengenai gerbang logika dan analisa rangkaian logika	● Kuliah, diskusi dan tugas. [TM : 3 x (4 x 50")] [BM : 3 x (4 x 50")] [PT : 3 x (4 x 50")]	• Chatting dan diskusi dalam forum platform ITS • *Chat and discussion in ITS platform forum*	• Gerbang logika dan aljabar bolean: inverter, gerbang AND, OR, NAND, NOR, XOR, XNOR, fixed-function logic gates, operasi dan ekspresi Boolean,	**Tugas 2 / *Task 2:* 2.5** **Praktikum 1 / *Lab Work 1*: 10**

	berkaitan dengan rangkaian dasar gerbang logika *Students are able to understand and explain about logic gates, Boolean algebra, simplification of logic equations and be able to do experiments related to basic logic gate circuits.*	perhitungan gerbang logika • Mampu menganalisa rangkaian logika • *Understand and be able to explain logic gates and Boolean algebra.* • *Able to solve logic gate calculations.* • *Able to analyze logic circuits.*	dasar, penyederhanaan persamaan logika (Tugas Tertulis) **Praktikum 1:** • Operasi gerbang logika dasar dan rangkaian logika dasar ***Non-test:*** ***Task 2:*** • *Solve calculation problems regarding logic gates and analysis of basic logic circuits, simplification of logic equations (Written Tasks)* ***Lab Work 1:*** • *Basic logic gate operations and basic logic circuits.*	• *Lectures discussion and assignment.* *[FF : 3 x (4 x 50")]* *[SS : 3 x (4 x 50")]* *[SA :3 x (4 x 50")]*		hukum dan aturan aljabar Boolean, teorema DeMorgan's, analisa Boolean pada rangkaian logika, bentuk standar dari ekpresi Boolean, ekpresi Boolean dan truth tables, karnaugh map (K-Map), SOP, POS • *Logic gates and boolean algebra: inverters, AND, OR, NAND, NOR, XOR, XNOR gates, fixed-function logic gates, Boolean operations and expressions, laws and rules of Boolean algebra, DeMorgan's theorem, Boolean analysis of logic circuits, standard form of Boolean expressions,*	

						Boolean expressions and truth tables, karnaugh map (K-Map), SOP, POS	
6, 7, 9	Mahasiswa mampu memahami, menjelaskan, merancang dan menganalisa rangkaian logika kombinasional serta mampu melakukan ekperimen berkaitan dengan rangkaian logika kombinasional *Students are able to understand, explain, design and analyze a combination of combinational logic and are able to experiment with a combination of combinational logic*	• Mengetahui dan mampu menjelaskan rangkaian logika kombinasional dan rangkaian fungsi logika kombinasional • Mampu menyelesaikan perhitungan mengenai analisa dan perancangan rangkaian kombinasional • Mampu menyelesaikan perhitungan mengenai analisa dan perancangan rangkaian fungsi logika kombinasional • *Know and be able to explain a series of combinational logic and a series of*	**Non-Tes:** **Tugas 4** • Mengerjakan soal perhitungan mengenai analisa dan perancangan rangkaian kombinasional dasar (Tugas Tertulis) **Tugas 5:** • Mengerjakan soal perhitungan mengenai analisa dan perancangan rangkaian fungsi logika kombinasional dan aplikasinya (Tugas Tertulis) **Praktikum 2:** • Rangkaian kombinasional dan penyederhanaan	• Kuliah, diskusi dan tugas. [TM : 3 x (4 x 50")] [BM : 3 x (4 x 50")] [PT : 3 x (4 x 50")] • *Lectures discussion and assignment.* *[FF : 3 x (4 x 50")]* *[SS : 3 x (4 x 50")]* *[SA :3 x (4 x 50")]*	• Chatting dan diskusi dalam forum platform ITS • *Chat and discussion in ITS platform forum*	• Rangkaian logika kombinasional : rangkaian dasar dan implementasi, gerbang universal (NAND dan NOR) dan implementasi, analisa rangkaian menggunakan timing diagram • Rangkaian fungsi logika kombinasional (decoder, encoder, multiplexer, demultiplexer, parity circuit, comparator, adder (H/A dan F/A), Arithmatic Logic Unit (ALU), multiplier) • Contoh aplikasi yang lain	**Tugas 4 / *Task 4*: 2.5** **Tugas 5 / *Task 5*: 2.5** **Praktikum 2 / *Lab work 2:* 10**

		functions of combinational logic. • *Able to solve calculations on combinational network analysis and designing.* • *Able to solve calculations on the analysis and design a combination of combinational logic functions*	rangkaian kombinasional ***Non-test:*** ***Task 4:*** • *Solve calculation problems regarding the analysis and design of basic combinational circuits (Written task)* ***Task 5:*** • *Solve calculation problems regarding the analysis and design of a series of combinational logic functions and their applications (written task)* ***Lab Work 2:*** • *Combinational circuits and combinational circuit simplification*			• *Combinational logic circuits: basic circuits and implementations, universal gates (NAND and NOR) and implementations, circuit analysis using timing diagrams* • *Combinational logic function circuit (decoder, encoder, multiplexer, demultiplexer, parity circuit, comparator, adder (H / A and F / A), Arithmatic Logic Unit (ALU), multiplier)* • *Other application example*	

8	**EVALUASI TENGAH SEMESTER** ***MID-SEMESTER EXAM***						**20**
10-12	Mahasiswa mampu memahami, menjelaskan, merancang dan menganalisa rangkaian logika sekuensial serta mampu melakukan ekperimen berkaitan dengan rangkaian logika sekuensial. *Students are able to understand, explain, design and analyze sequential logic circuits and be able to do experiments related to sequential logic circuits*	• Mampu melakukan perhitungan, merancang dan menganalisa rangkaian bistable, rangkaian monostable (one shot), rangkaian astable. • Mampu melakukan perhitungan, merancang dan menganalisa Latch, flip-flop, register, counter. • Mampu melakukan perhitungan, merancang dan menganalisa sistem digital menggunakan FSM. • *Able to solve calculations, design and analyze bistable circuits, monostable circuits (one shot), astable circuits.*	**Non tes:** **Tugas 6:** • Mengerjakan soal perhitungan mengenai analisa dan perancangan rangkaian bistable, rangkaian monostable (one shot), rangkaian astable, latch, flip-flop, register, counter serta mencari contoh aplikasinya (Tugas Tertulis) **Tugas 7:** • Mengerjakan soal perhitungan mengenai analisa dan perancangan sistem digital menggunakan FSM (Tugas Tertulis) **Praktikum 3:**	• Kuliah, diskusi dan tugas. [TM : 3 x (4 x 50")] [BM : 3 x (4 x 50")] [PT : 3 x (4 x 50")] • *Lectures discussion and assignment.* *[FF : 3 x (4 x 50")]* *[SS : 3 x (4 x 50")]* *[SA :3 x (4 x 50")]*	• Chatting dan diskusi dalam forum platform ITS • *Chat and discussion in ITS platform forum*	• Rangkaian bistable, rangkaian monostable (one shot), rangkaian astable • Latch, flip-flop, *register, counter* • *finite state machine* (FSM) : perancangan dan analisa sistem digital menggunakan FSM) • Contoh aplikasi yang lain • *Bistable circuit, monostable circuit (one shot), astable circuit* • *Latch, flip-flop, register, counter* • *finite state machine (FSM): design and analysis of digital systems using FSM)*	**Tugas 6 / *Task 6*: 2.5** **Tugas 7 / *Task 7:* 2.5** **Praktikum 3 / *Lab work 3*: 10**

		• *Able to solve calculations, design and analyze Latch, flip-flops, registers, counters.* • *Able to solve calculations, design and analyze digital systems using FSM.*	• Rangkaian sekuensial ***Non-test:*** ***Task 6:*** • *Solve calculation problems regarding the analysis and design of bistable circuits, monostable circuits (one shot), astable circuits, latches, flip-flops, registers, counters and looking for examples of their application (Written task)* ***Task 7:*** • *Solve calculation problems regarding digital system analysis and design using FSM (Written task)*			• *Other application examples*	

			Lab work 3: • *Sequential circuit*				
13-15	Mahasiswa mampu memahami dan menjelaskan tahapan perancangan sistem digital berbasis Programmable Logic Device (PLD) serta mampu merealisasikannya *Students are able to understand and explain the stages of designing a digital-based Programmable Logic Device (PLD) system and be able to realize it.*	• Mengetahui dan mampu menjelaskan mengenai *Programmable Logic Device (PLD) dan Hardware Description Language (HDL)* • Mampu menganalisa dan merancang sistem digital berbasis PLD (Tugas Tertulis) • *Know and be able to explain about Programmable Logic Device (PLD) and Hardware Description Language (HDL).* • *Able to analyze and design PLD-based digital systems (Written Assignments).*	**Non-tes :** **Tugas 8:** • Mengerjakan soal mengenai analisa dan perancangan sistem digital berbasis PLD (Tugas Tertulis). **Praktikum 4:** • Perancangan sistem digital berbasis PLD ***Non-test:*** ***Task 8:*** • *Solve questions regarding the analysis and design of a PLD-based digital system (Written Task).* ***Lab work 4:*** • *PLD-based digital system design*	● Kuliah, diskusi dan tugas. [TM : 3 x (4 x 50")] [BM : 3 x (4 x 50")] [PT : 3 x (4 x 50")] ● *Lectures discussion and assignment.* *[FF : 3 x (4 x 50")]* *[SS : 3 x (4 x 50")]* *[SA :3 x (4 x 50")]*	• Chatting dan diskusi dalam forum platform ITS • *Chat and discussion in ITS platform forum*	• *Programmable Logic Device (PLD)* dan *Hardware Description Language (HDL) : SPLD, CPLD, FPGA, Programmable Logic software, VHDL* • *Programmable Logic Device (PLD) and Hardware Description Language (HDL) : SPLD, CPLD, FPGA, Programmable Logic software, VHDL*	**Tugas 8 / Task 8: 2.5** **Praktikum 4 / Lab work 4: 10**

16	**EVALUASI AKHIR SEMESTER** ***FINAL-SEMESTER EXAM***	**20**

TM=Tatap Muka, **PT**=Penugasan Terstuktur, **BM**=Belajar MandirI.
***FF** = Face to Face, **SA** = Structured Assignment, **SS** = Self Study.*

II. Rencana Asesmen & Evaluasi (RAE)/ *Assessment & Evaluation Plan*

	ASSESSMENT & EVALUATION PLAN BACHELOR DEGREE PROGRAM OF BIOMEDICAL ENGINEERING - FTEIC ITS **Course : Digital Techniques and Laboratory**		**RA&E** Write Doc Code
Kode/*code*: **EW184405**	**Bobot sks/*credits* (T/P): 4/0**	**Rumpun MK: Biomedical Instrumentation and Signal Processing** ***Course Cluster: Biomedical Instrumentation and Signal Processing***	Smt: IV
OTORISASI ***AUTHORIZATION***	**Penyusun RA & E** ***Compiler A&EP*** **Dr. Tri Arief Sardjono, S.T., M.T.**	**Koordinator RMK** ***Course Cluster Coordinator*** **Dr. Rachmad Setiawan, S.T., M.T.**	**Ka DEP** ***Head of DEP*** **Dr. Achmad Arifin, S.T., M.Eng.**

Mg ke/ *Week* (1)	**Sub CP-MK / *Lesson Learning Outcomes (LLO)* (2)**	**Bentuk Asesmen (Penilaian) *Form of Assessment* (3)**	**Bobot / *Load* (%) (4)**
1,2	**Sub CP-MK 1:** Mahasiswa mampu memahami dan menjelaskan teori dasar sistem elektronika digital seperti perbedaan antara sistem analog dan sistem digital, sistem bilangan dan sistem pengkodean. ***LLO 1:*** *Students are able to understand and explain basic theories of digital electronic systems such as the difference between analog systems and digital systems, number systems and coding systems..*	**Non-tes:** **Tugas 1** Mengerjakan soal perhitungan mengenai konversi bilangan, aritmatika biner, komplemen bilangan biner, bilangan bertanda dan operasinya, dan sistem pengkodean (Tugas Tertulis) **Tes:** ETS Soal 1 (6% dari ETS 20%) ***Non-Test*** ***Task 1:*** *Doing calculation problems about number conversion, binary arithmetic, binary number complement, marked numbers and their operations, and coding systems (Written Tasks)* ***Test:*** *Question 1 in Mid Exam (6% of Mid Exam 20%)*	Tugas 1 / *Task 1:* 2.5

3-5	**Sub CP-MK 2:** Mahasiswa mampu memahami dan menjelaskan tentang gerbang logika, aljabar boolean, penyederhanaan persamaan logika serta mampu melakukan ekperimen berkaitan dengan rangkaian dasar gerbang logika. ***LLO 2:*** *Students are able to understand and explain about logic gates, Boolean algebra, simplification of logic equations and be able to do experiments related to basic logic gate circuits.*	**Non-tes :** **Tugas 2:** Mengerjakan soal perhitungan mengenai gerbang logika dan analisa rangkaian logika dasar, penyederhanaan persamaan logika (Tugas Tertulis) **Praktikum 1:** Operasi gerbang logika dasar dan rangkaian logika dasar **Tes :** ETS Soal 2 (7% dari ETS 20%) ***Non-test:*** ***Task 2:*** *Solve calculation problems regarding logic gates and analysis of basic logic circuits, simplification of logic equations (Written Tasks)* ***Lab Work 1:*** *Basic logic gate operations and basic logic circuits..* ***Test:*** • *Question 2 in Mid Exam (7% of Mid Exam 20%)*	Tugas 2 / *Task 2:* 2.5 Praktikum 1 / *Lab Work 1:* 10
6, 7, 9	**Sub CP-MK 3:** Mahasiswa mampu memahami, menjelaskan, merancang dan menganalisa rangkaian logika kombinasional serta mampu melakukan ekperimen berkaitan dengan rangkaian logika kombinasional. ***LLO 3:*** *Students are able to understand, explain, design and analyze a combination of combinational logic and are able to*	**Non-Tes:** **Tugas 4** Mengerjakan soal perhitungan mengenai analisa dan perancangan rangkaian kombinasional dasar (Tugas Tertulis) **Tugas 5:** Mengerjakan soal perhitungan mengenai analisa dan perancangan rangkaian fungsi logika kombinasional dan aplikasinya (Tugas Tertulis) **Praktikum 2:** Rangkaian kombinasional dan penyederhanaan rangkaian kombinasional **Tes :** ETS Soal 3 (7% dari ETS 20%) ***Non-test:*** ***Task 4:***	Tugas 4 / *Task 4:* 2.5 Tugas 5 / *Task 5:* 2.5 Praktikum 2 / *Lab work 2:* 10

	experiment with a combination of combinational logic.	*Solve calculation problems regarding the analysis and design of basic combinational circuits (Written task)* ***Task 5:*** *Solve calculation problems regarding the analysis and design of a series of combinational logic functions and their applications (written task)* ***Lab Work 2:*** *Combinational circuits and combinational circuit simplification* ***Test:*** *Question 3 in Mid Exam (7% of Mid Exam 20%)*	
8	**Evaluasi Tengah Semester** ***Mid Exam***	**Tes:** Ujian Tulis/Ujian Daring ***Test:*** *Writing Exams / Online Exams*	20
10-12	**Sub CP-MK 4:** Mahasiswa mampu memahami, menjelaskan, merancang dan menganalisa rangkaian logika sekuensial serta mampu melakukan ekperimen berkaitan dengan rangkaian logika sekuensial. ***LLO 4:*** *Students are able to understand, explain, design and analyze sequential logic circuits and be able to do experiments related to sequential logic circuits.*	**Non tes:** **Tugas 6:** Mengerjakan soal perhitungan mengenai analisa dan perancangan rangkaian bistable, rangkaian monostable (one shot), rangkaian astable, latch, flip-flop, register, counter serta mencari contoh aplikasinya (Tugas Tertulis) **Tugas 7:** Mengerjakan soal perhitungan mengenai analisa dan perancangan sistem digital menggunakan FSM (Tugas Tertulis) **Praktikum 3:** Rangkaian sekuensial. **Tes :** EAS Soal 1 (10% dari EAS 20%) ***Non-test:*** ***Task 6:*** *Solve calculation problems regarding the analysis and design of bistable circuits, monostable circuits (one shot), astable circuits, latches, flip-flops, registers, counters and looking for examples of their application (Written task)* ***Task 7:*** *Solve calculation problems regarding digital system analysis and design using FSM (Written task)*	Tugas 6 / *Task 6:* 2.5 Tugas 7 / *Task 7:* 2.5 Praktikum 3 / *Lab work 3:* 10

		Lab work 3: *Sequential circuit* ***Test:*** *Question 1 in Final Exam (10% of Mid Exam 20%)*	
13-15	**Sub CP-MK 5:** Mahasiswa mampu memahami dan menjelaskan tahapan perancangan sistem digital berbasis Programmable Logic Device (PLD) serta mampu merealisasikannya. ***LLO 5:*** *Students are able to understand and explain the stages of designing a digital-based Programmable Logic Device (PLD) system and be able to realize it.*	**Non-tes :** **Tugas 8:** Mengerjakan soal mengenai analisa dan perancangan sistem digital berbasis PLD (Tugas Tertulis). **Praktikum 4:** Perancangan sistem digital berbasis PLD **Tes :** EAS Soal 2 (17.5% dari EAS 35%) ***Non-test:*** ***Task 8:*** *Solve questions regarding the analysis and design of a PLD-based digital system (Written Task).* ***Lab work 4:*** *PLD-based digital system design* ***Test:*** *Question 2 in Final Exam (12.5% of Final Exam 20%)*	Tugas 8 / *Task 8:* 2.5 Praktikum 4 / *Lab work 4:* 10
16	**Evaluasi Akhir** ***Final Exam***	**Tes:** Ujian Tulis/Ujian Daring ***Test:*** *Writing Exams / Online Exams*	20
		Total bobot penilaian ***Total assessment load***	**100%**

Indikator Pencapaian CPL Pada MK / *Indicator of PLO achievement charged to the course*

CPL yang dibebankan pada MK / *PLO charged to the course*	CPMK / *Course Learning Outcome (CLO)*	Minggu ke / *Week*	Bentuk Asesmen / *Form of Assessment*	Bobot / *Load* (%)
CPL-02 / *PLO-02*	CPMK 1 / *CLO 1*	*Week- 1-2*	*Task 1*	2.5
		Week- 8	*Mid Exam question 1*	6
CPL-03 / *PLO-03*	CPMK 2 / *CLO 2*	*Week- 3-5*	*Task 2*	2.5
			Lab Work 1	10
		Week- 8	*Mid Exam question 2*	7
	CPMK 3	*Week- 6,7,9*	*Task 4*	2.5
			Task 5	2.5
			Lab Work 2	10
		Week- 8	*Mid Exam question 3*	7
	CPMK 4	*Week- 10-12*	*Task 6*	2.5
			Task 7	2.5
			Lab Work 3	10
		Week- 16	*Final Exam question 1*	10
CPL-05 / PLO-05	CPMK 5	*Week- 13-15*	*Task 8*	2.5
			Lab Work 4	10
		Week- 16	*Final Exam question 2*	12.5
				∑ = 100%

No	*Form of Assessment*	*PLO-01*	*PLO-02*	*PLO-03*	*PLO-04*	*PLO-05*	*PLO-06*	*PLO-07*	*PLO-08*	*PLO-09*	*PLO-10*	*PLO-11*	*PLO-12*	*Total*
1	*Task 1*		0.025											**0.025**
2	*Task 2*			0.025										**0.025**
3	*Task 4*			0.025										**0.025**

4	*Task 5*			0.025										**0.025**
5	*Task 6*			0.025										**0.025**
6	*Task 7*			0.025										**0.025**
7	*Task 8*					0.025								**0.025**
8	*Lab work 1*			0.1										**0.1**
9	*Lab work 2*			0.1										**0.1**
10	*Lab work 3*			0.1										**0.1**
11	*Lab work 4*					0.1								**0.1**
12	*Mid Exam*		0.06	0.14										**0.2**
13	*Final Exam*			0.1		0.125								**0.225**
	Total		0.085	0.665		0.25								**1**