Module name	**Programmable Devices**
Module level	Undergraduate
Code	EC184913
Courses (if applicable)	Programmable Devices
Semester	Elective
Contact person	Ahmad Zaini, ST . MT
Lecturer	Ahmad Zaini, ST . MT
Language	Indonesia / English
Relation to curriculum	Undergraduate degree program, *elective* semester.
Type of teaching, contact hours	Lecture, < 60 students, 170 Minute 3 SKS
Workload	1. *Lectures: 3x 50 = 150 minutes (2.5 hours) per week.* 2. *Exercises and Assignments: 3 x 60 = 180 minutes (3 hours) per week.* 3. *Private study: 3 x 60 = 180 minutes (3 hours) per week.*
Credit points	3 credit points (sks).
Requirements according to the examination regulations	A student must have attended at least 75% of the lectures to sit in the exams.
Mandatory prerequisites	• Basic Computer Programming • Digital Circuits and Laboratory • Electronic Circuits • Digital Signal Processing
Learning outcomes and their corresponding PLOs	CLO-1 Students are able to explain the digital circuits and systems for design and classification techniques, evolution of programmable H/W components, internal architecture of programmable H/W components such as PLD and FPGA and their respective advantages and disadvantages.	PLO-3 PLO-4
	CLO-2 Students are able to master the design stage of digital system based on H/W programmable ranging from the desired specification stage to testing stage	PLO-3 PLO-4
	CLO-3 Student ara able to design a simple digital system based H/W programmable with the correct methodology	PLO-5

	CLO-4 Student are able to understand the verification techniques and their usage.	PLO-6
Content	In this course, students will learn about the principles and practices in design of digital devices and digital systems using VHDL and Fieldprogrammable gate array	
Study and examination requirements and forms of examination	• *In-class exercises* • *Quiz 1 and 2* • *Assignment 1, 2, 3* • *Mid-term examination* • *Final examination*	
Media employed	*LCD, whiteboard, websites (myITS Classroom).*	
Assessments and Evaluation	*CO-1: Question no 1 in midterm exam (10%)* *CO-2: Question no 2 in midterm exam (10%)* *CO-3: Assignment 1 (5%), question no 4 in midterm exam (20%), Quiz 2 (5%)* *CO-4: Question no 1 in final exam (25%), question no 2 in final exam (25%)*	
Reading List	1. "The VHDL Cookbook", Peter J Andensen, 1st Edition, 1990. 2. "Digital System Design With VHDL and Synthesis", K.C. Chang, Computer Society, 1999.	